Arquitectura y software Intel optimizados para GRID y HPC

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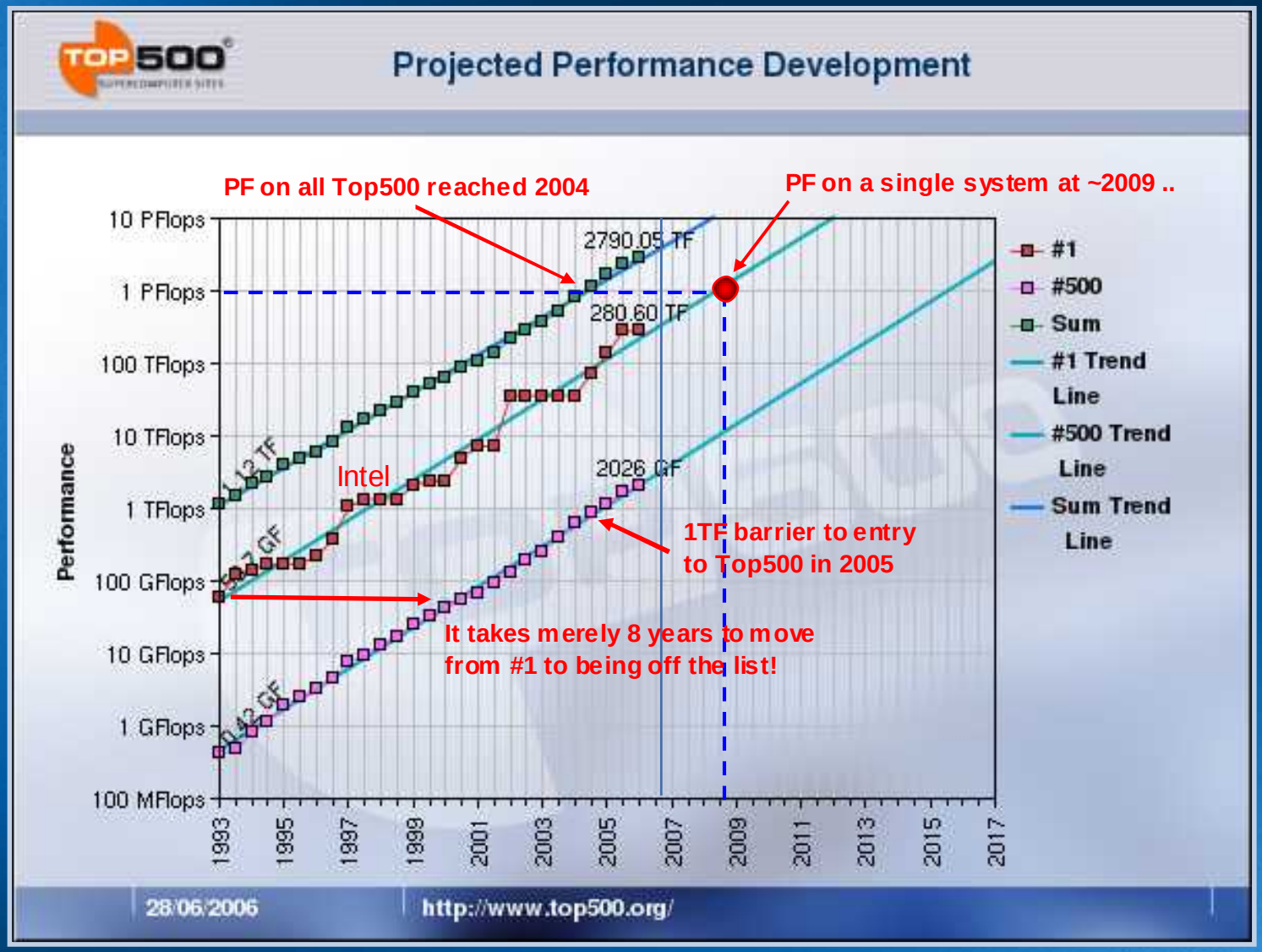

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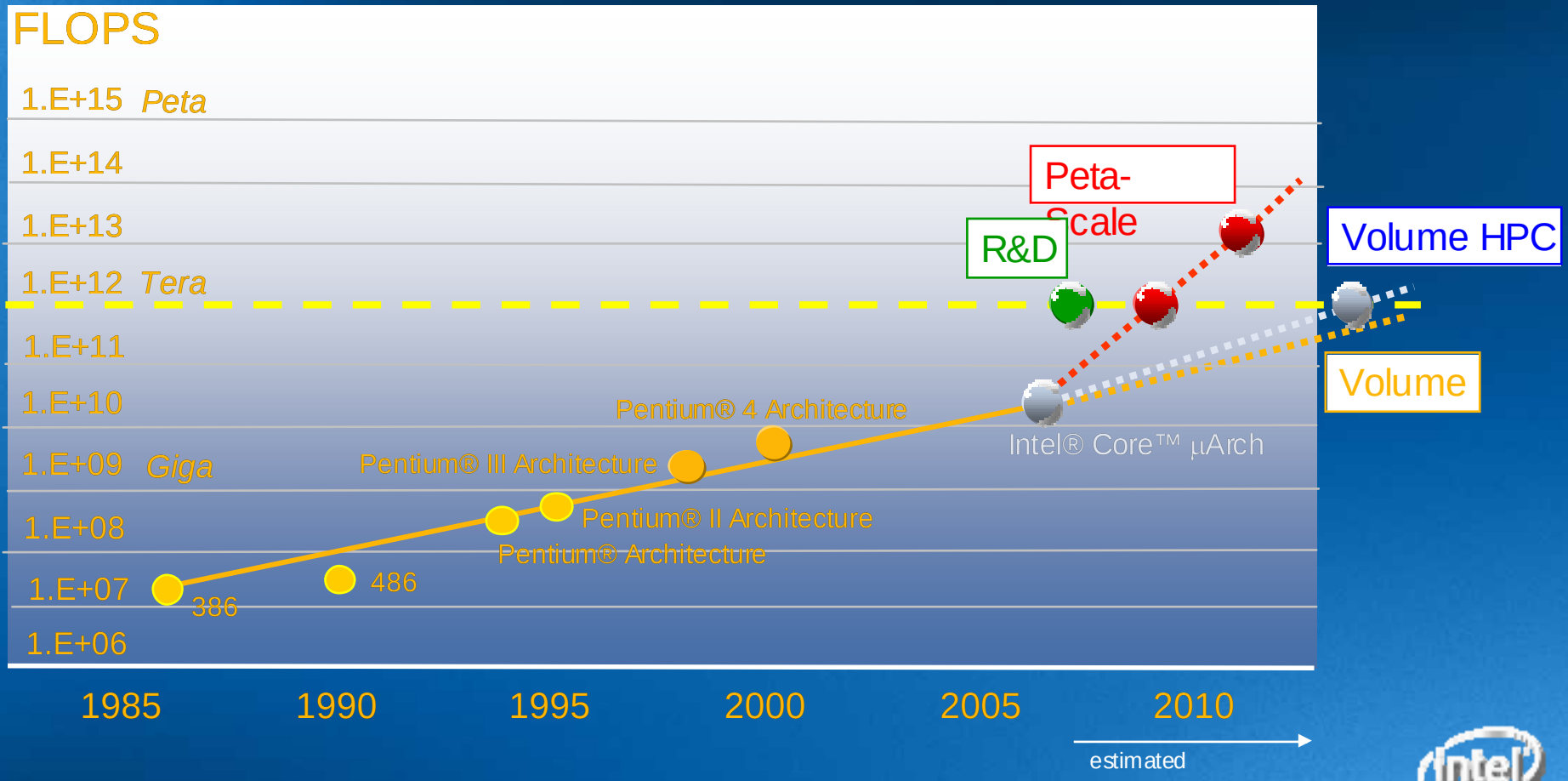
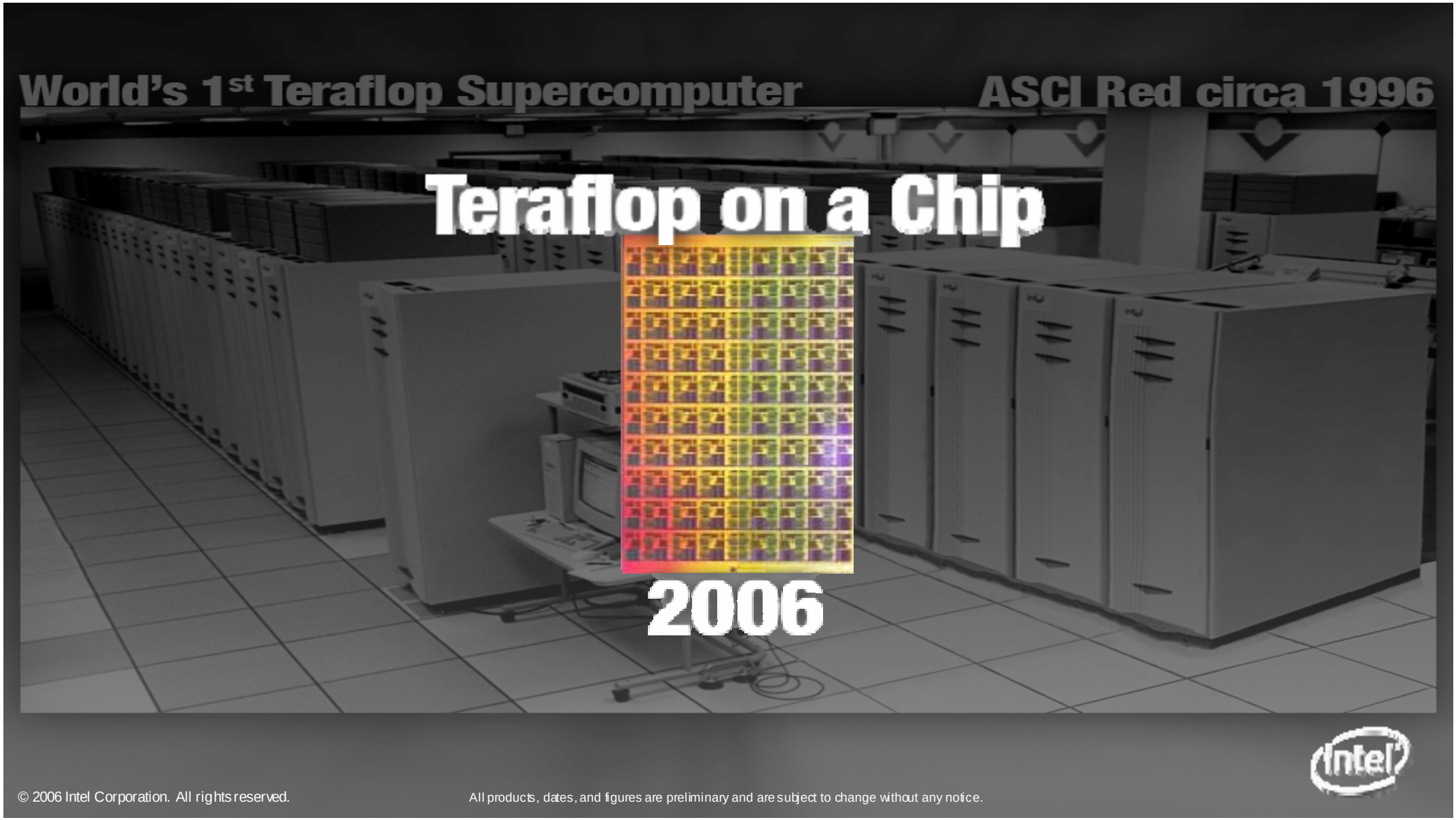
Increasing Processor Performance
Through Multi-Threaded Cores



Future options subject to change without notice. Source: Intel

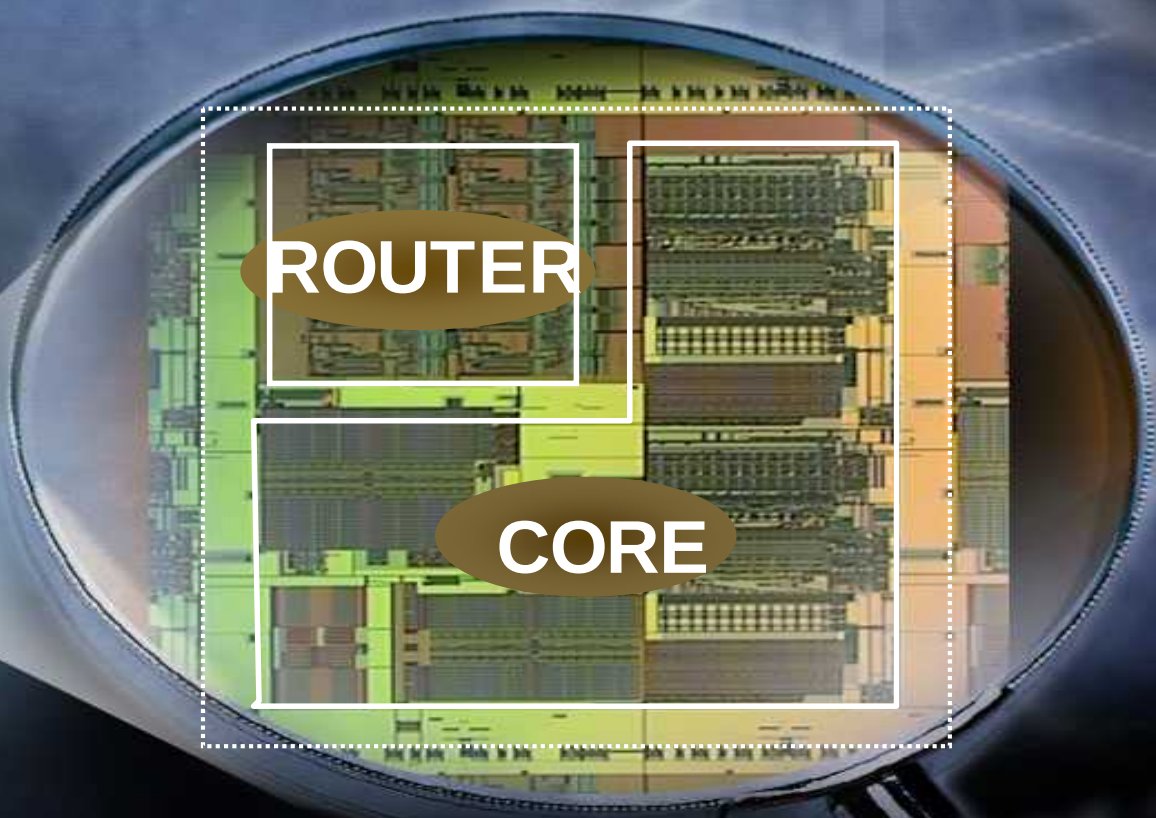
World's 1st Teraflop Supercomputer

ASCI Red circa 1996



All products, dates, and figures are preliminary and are subject to change without any notice.

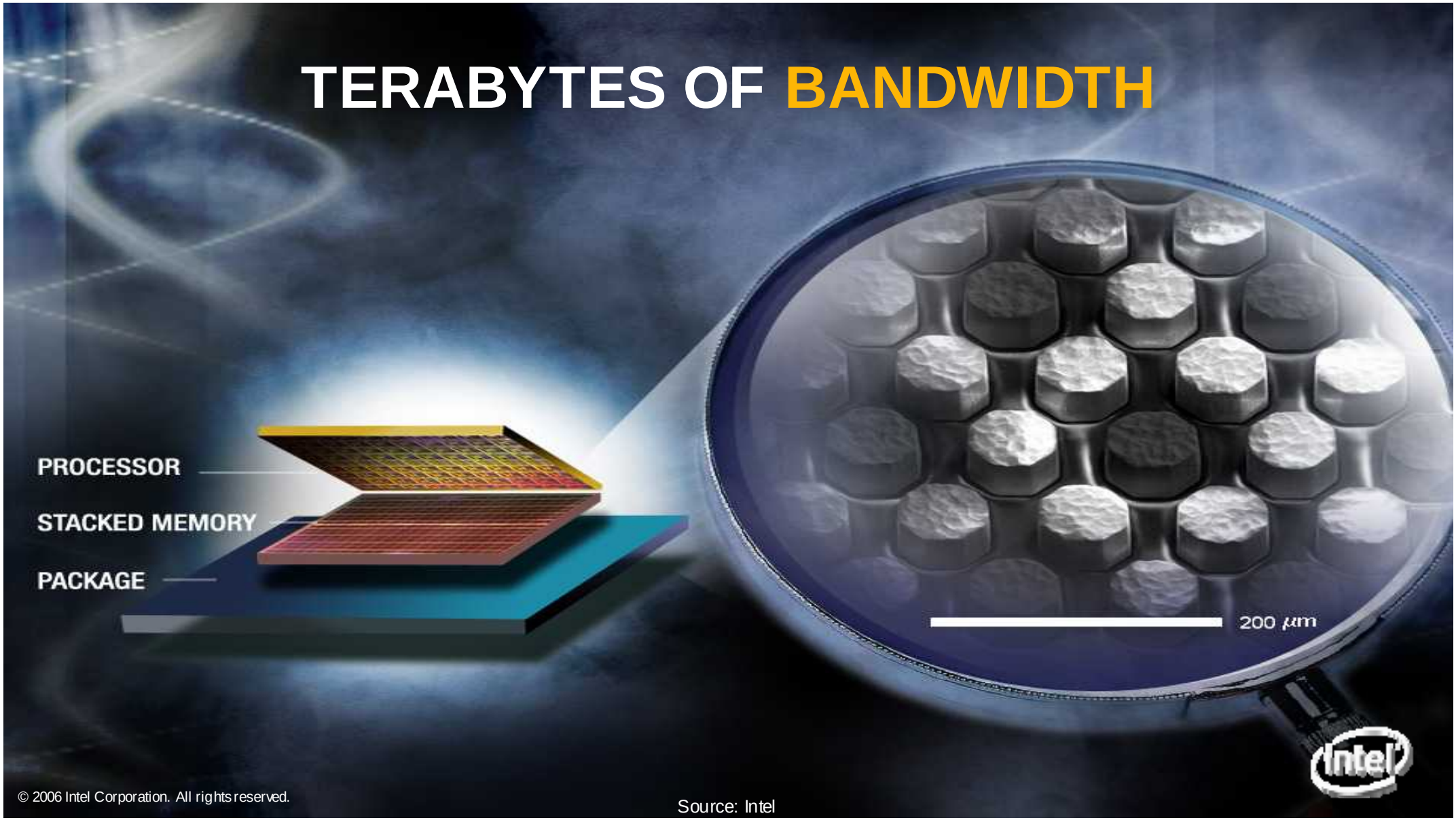
TERAFLOP OF PERFORMANCE



Experimental Research Prototype

Source: Intel

TERABYTES OF BANDWIDTH



Source: Intel

TERABITS OF I/O-THROUGHPUT

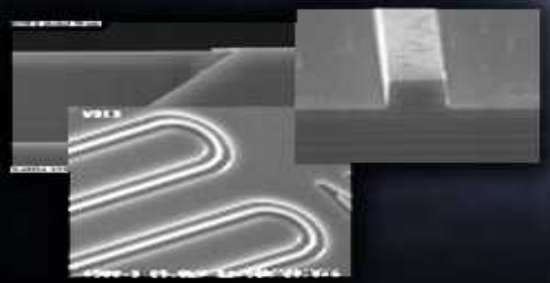
LASER

MODULATOR

PHOTO-DETECTOR

LOGIC INTEGRATION

LIGHT GUIDES



SELF-ALIGNMENT

BUILDING BLOCKS OF SILICON PHOTONICS

Source: Intel

IA: Architectural Choice & Flexibility

- Mainframes
- Large SMPs
- Constellations

Itanium 2 inside

Xeon inside

Core 2 Duo inside

- MPP
- Clusters
- Personal Clusters

Full Range of HPC System Architectures

Source: courtesy of SGI

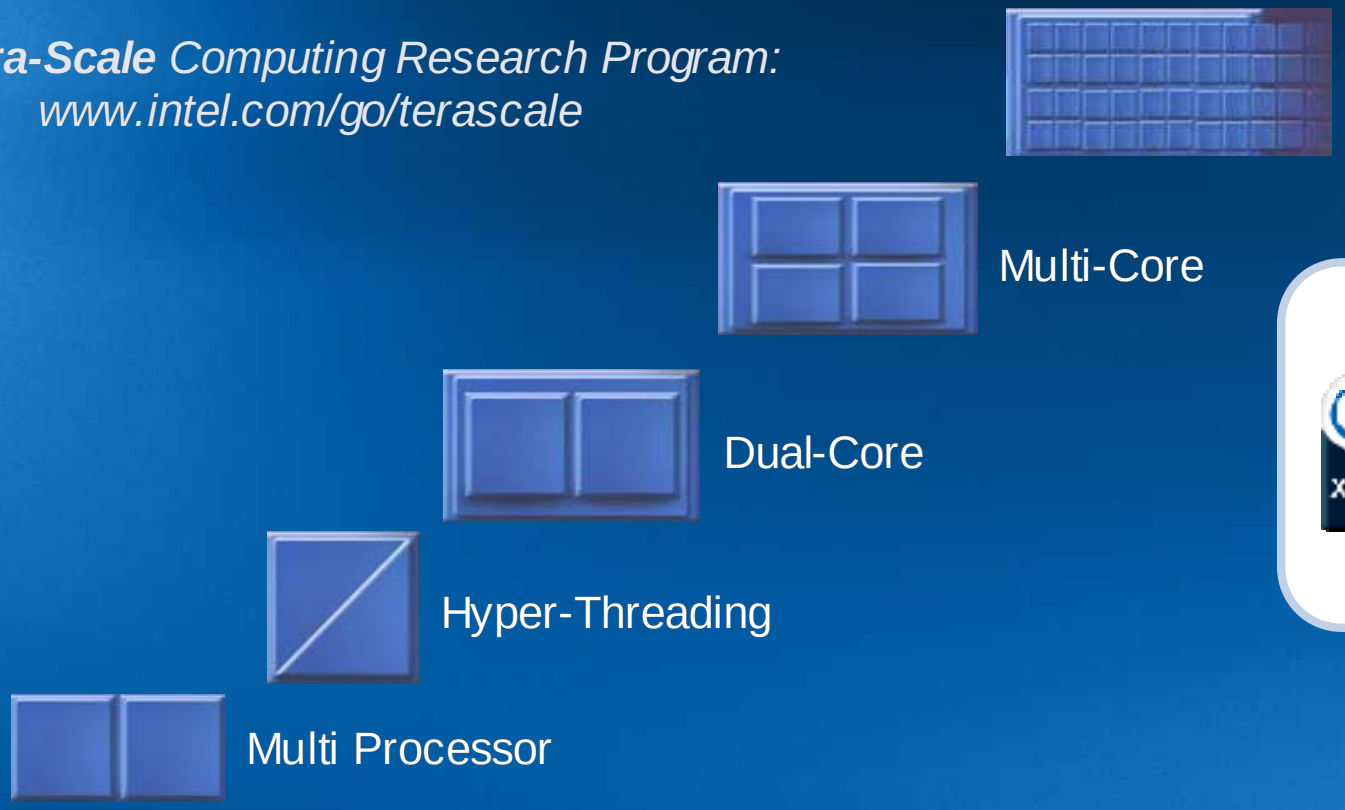
Source: courtesy of BULL

Shared Memory
(SMP scale-up)

Distributed Memory
(Cluster scale-out)

Industry Trend to Multi/Many-Core

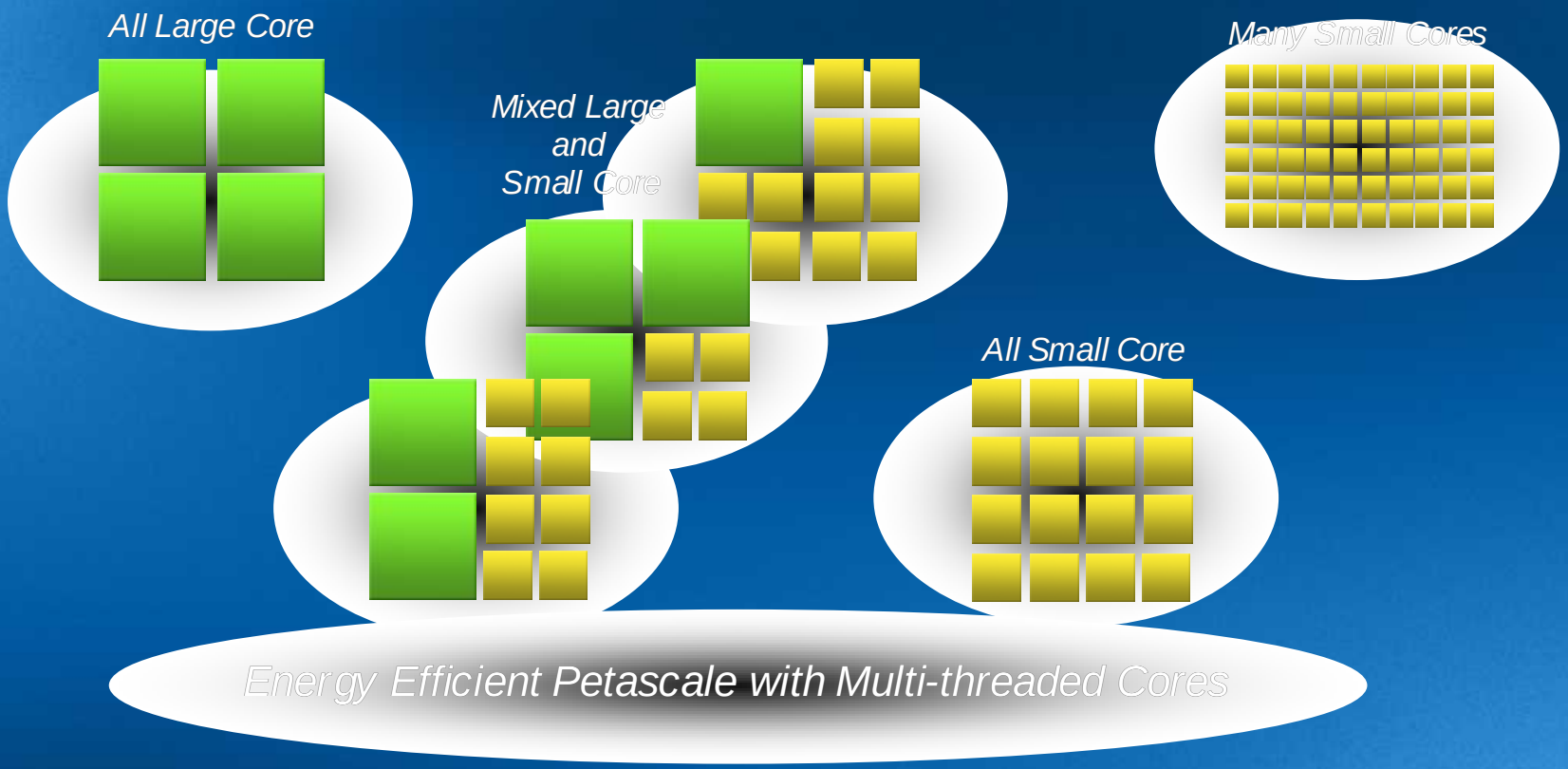
*Intel **Tera-Scale** Computing Research Program:*
www.intel.com/go/terascale



Energy Efficient Petascale with Multi-threaded Cores

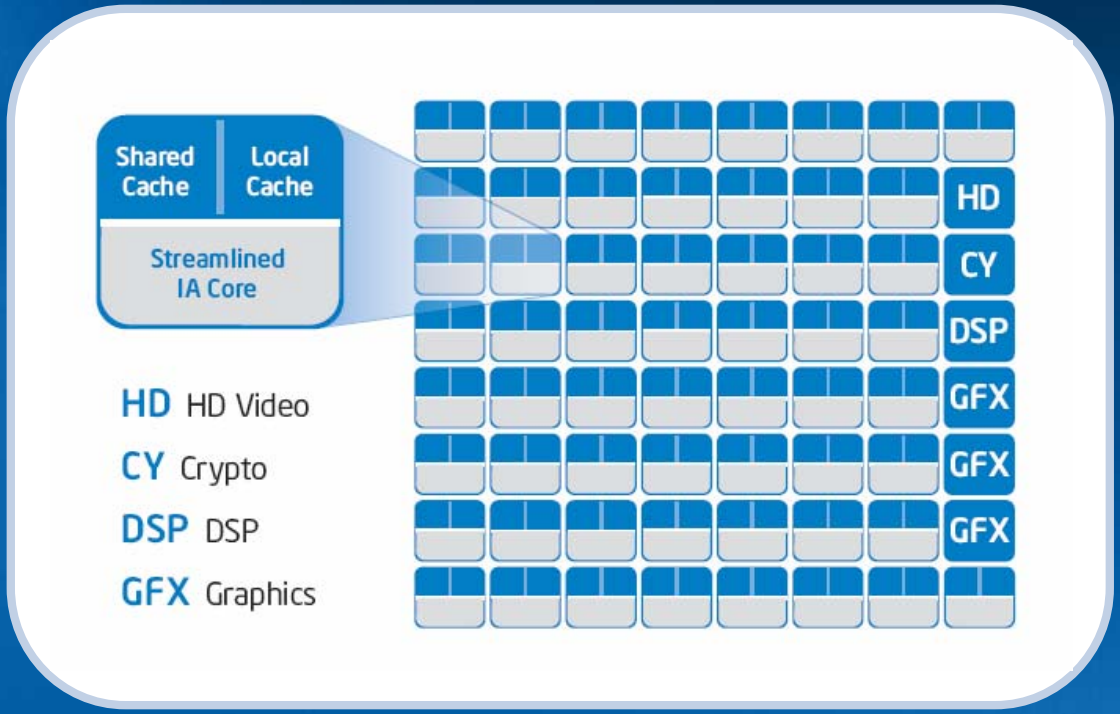
Multi-Threaded Cores

*Intel **Tera-Scale** Computing Research Program:*
www.intel.com/go/terascale



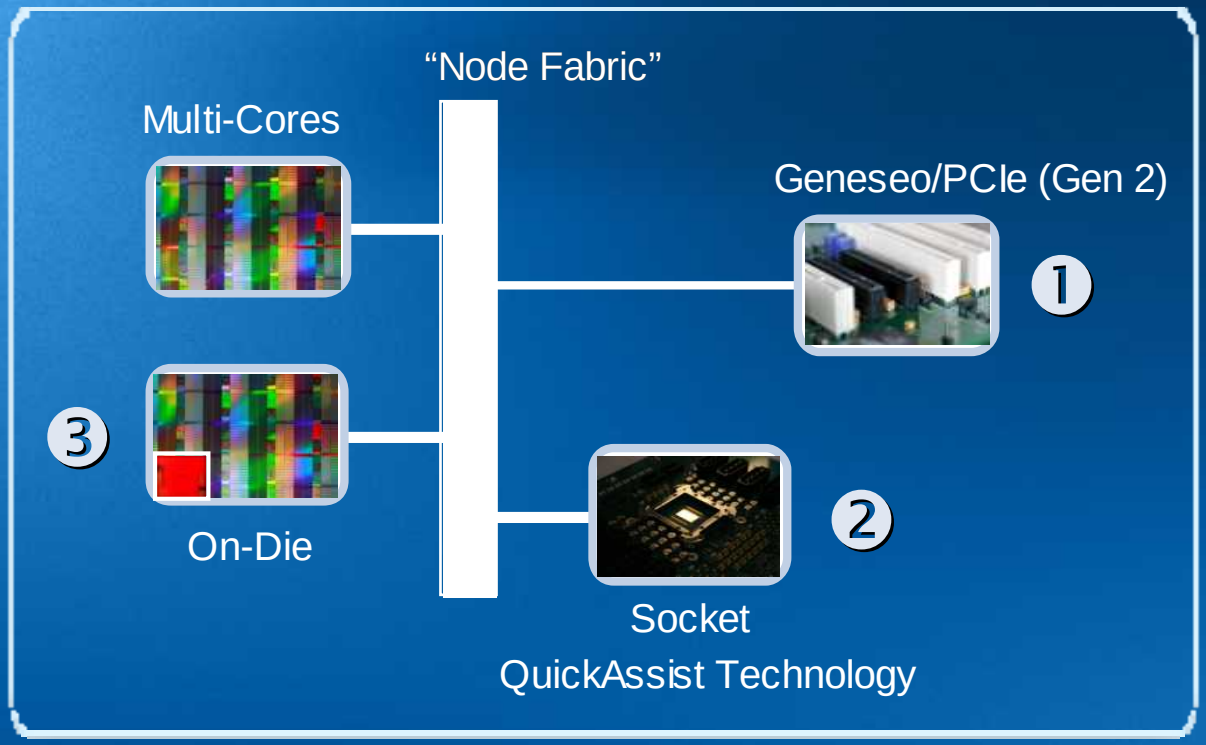
Note: the above pictures don't represent any current or future Intel products

Multi/Many-Core Chip Research



Future tera-scale chips could use an array of tens to hundreds of cores with reconfigurable caches, as well as special-purpose hardware accelerators utilizing a scalable on-die interconnect fabric.

Potential HW-Accelerator Options



Enabling Partnerships

Intel® QuickAssist Technology

Encompasses Industry Hardware Solutions

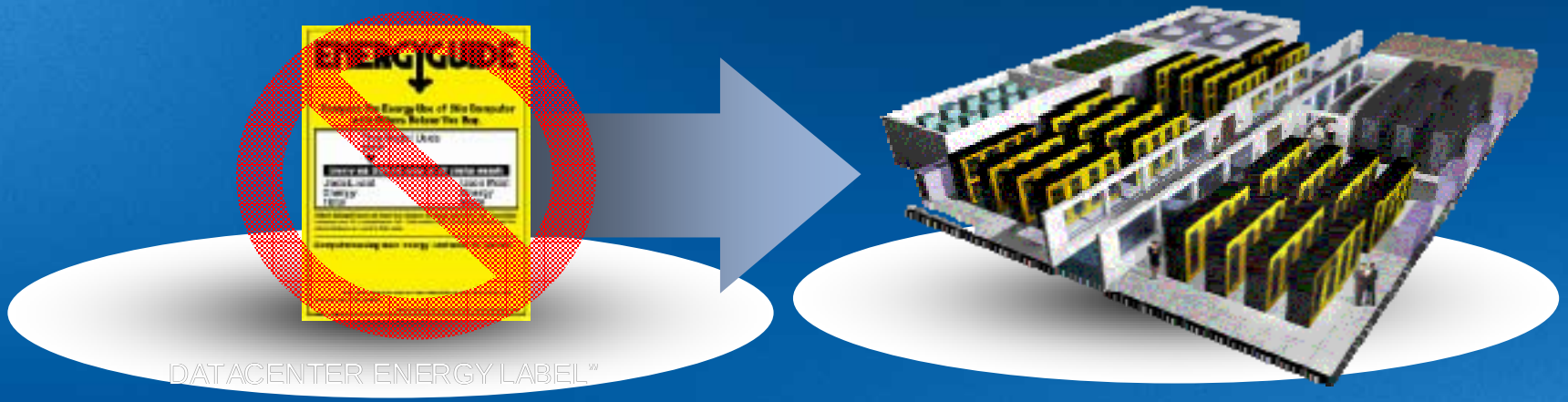
Future Intel Processor Integration of Accelerators

Software Architecture Abstraction Layer and Libraries For Acceleration

Comprehensive Approach To Acceleration

Power and Cooling Cost Today

10¢ *Kilowatt Hour* + **9** *Megawatt Datacenter* + *Power Delivery + Cooling* = **$14.6M** *Electricity Costs/Year*



Assume: 9MW system power*, 90% power delivery efficiency, cooling Co-efficiency of Performance (COP)=1.5

*Source: HPC Wire "A Petaflop Before its Time," June 28, 2006

Commitment to Energy Efficiency

Data Source: Intel measured results as of Feb. 27, 2006

Intel's Software Tools and Support for Parallelism

Intel® Thread Checker
Intel® Thread Profiler
Intel® Threading Building Blocks

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Intel's Software Tools and Support for HPC

Intel® Cluster Toolkit

Performance | Compatibility | Support | Productivity | Cross-Platform

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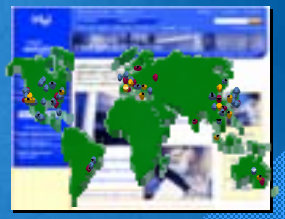
Intel HPC Products and Services

User Needs

Intel R&D



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your Performance
with Ease

Processors

Chipsets

Validation

High Density Intel Platforms

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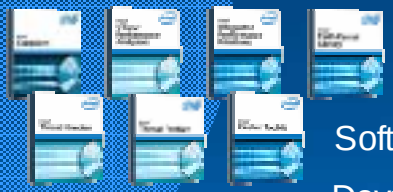
Boards & Server Systems

Communication & Storage
Building Blocks

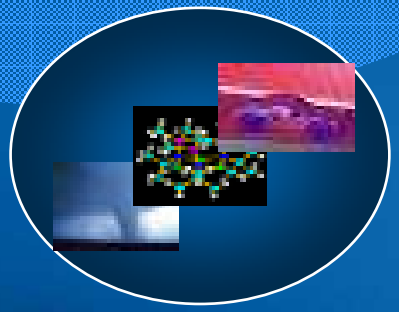


Software Tools

Developer Services

Industry Standards

Collaborations &
User Engagements



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Early Access Program

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